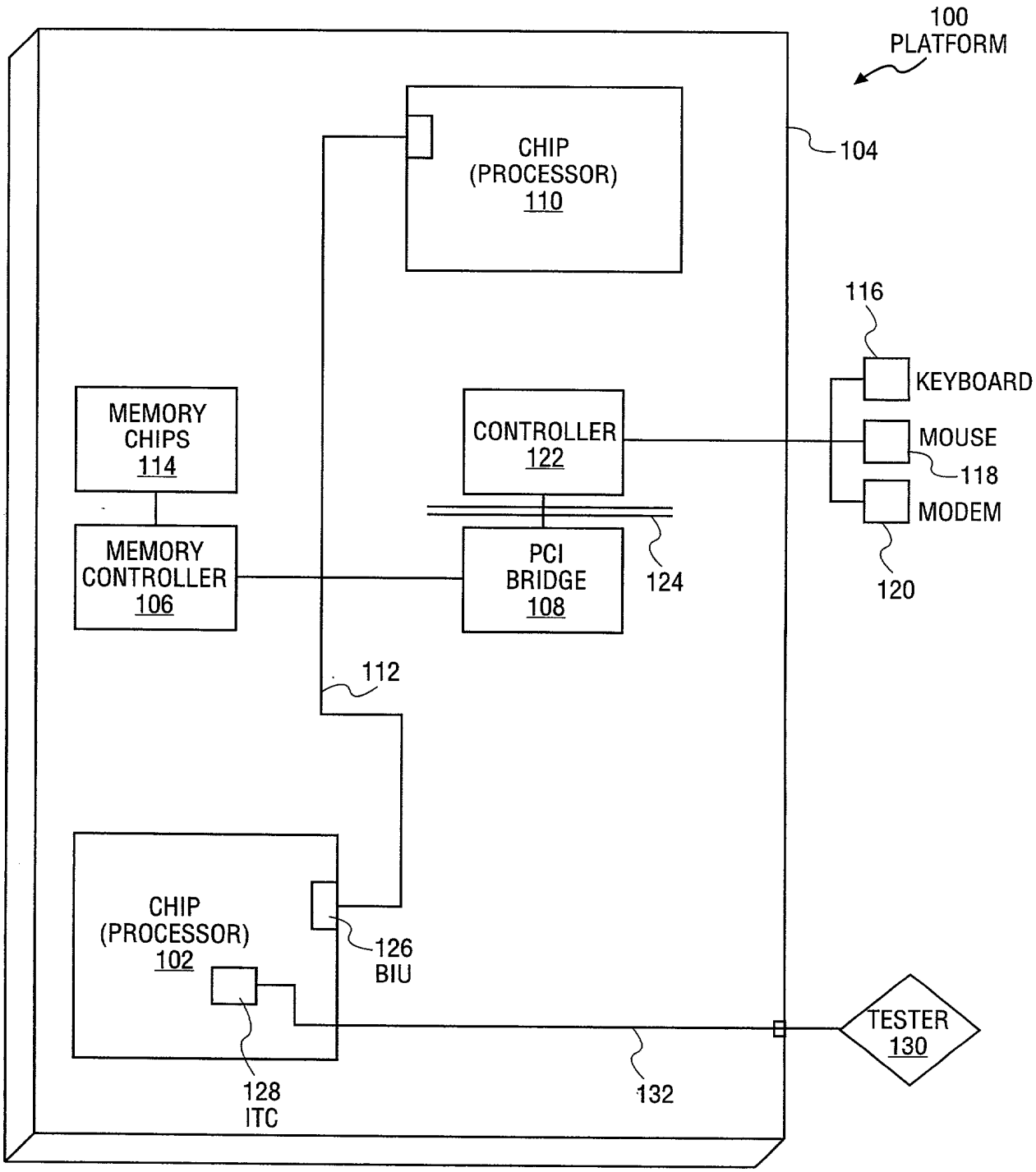
100
PLATFORM
CHIP
(PROCESSOR)
110
104
116
KEYBOARD
MOUSE
118
MODEM
120
MEMORY
CHIPS
114
CONTROLLER
122
MEMORY
CONTROLLER
106
PCI
BRIDGE
108
124
112
CHIP
(PROCESSOR)
102
126
BIU
TESTER
130
128
ITC
132

FIG. 1

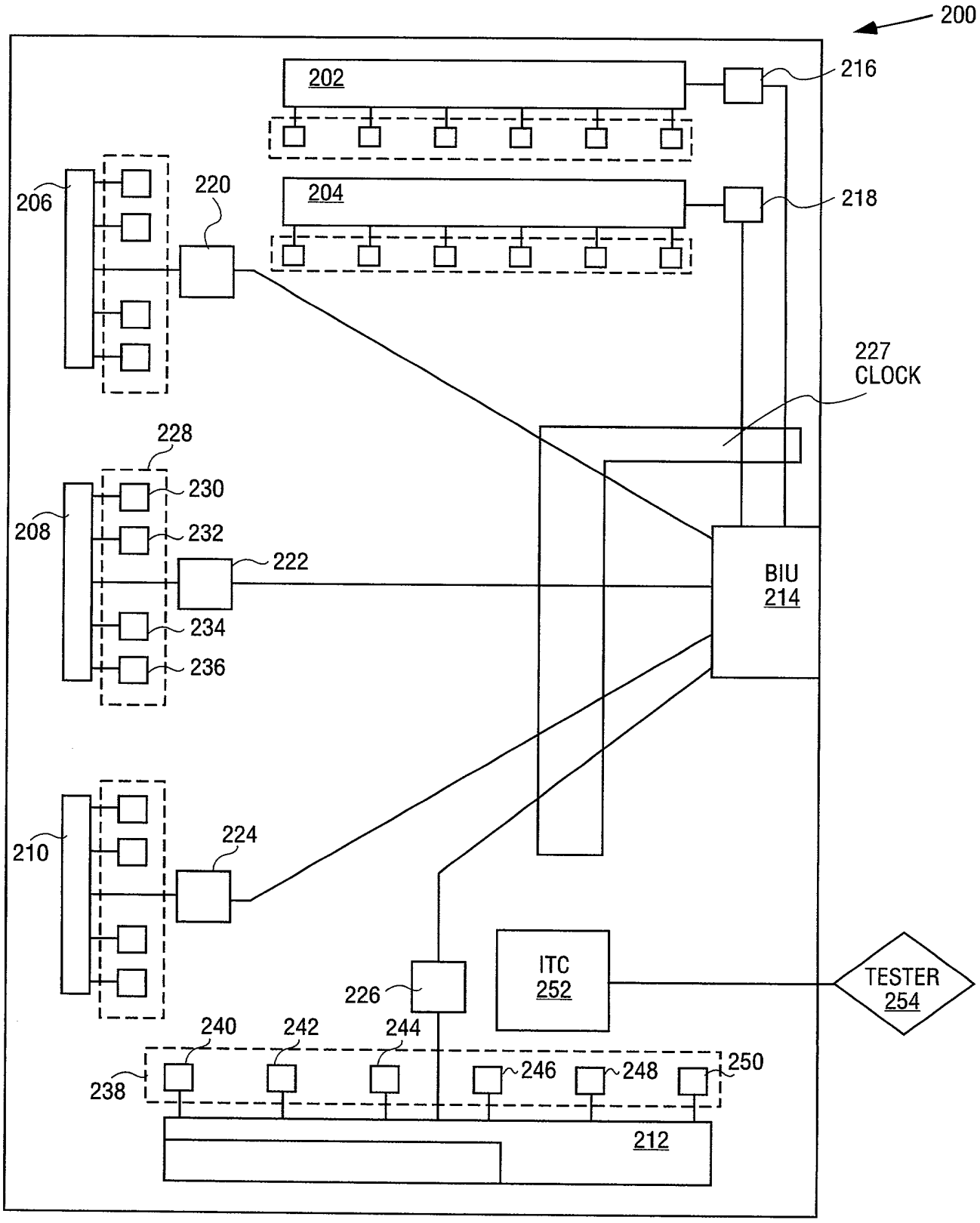
200
202
216
204
218
206
220
227
CLOCK
228
230
208
232
222
BIU
214
234
236
210
224
ITC
252
TESTER
254
226
240
242
244
246
248
250
238
212

FIG. 2

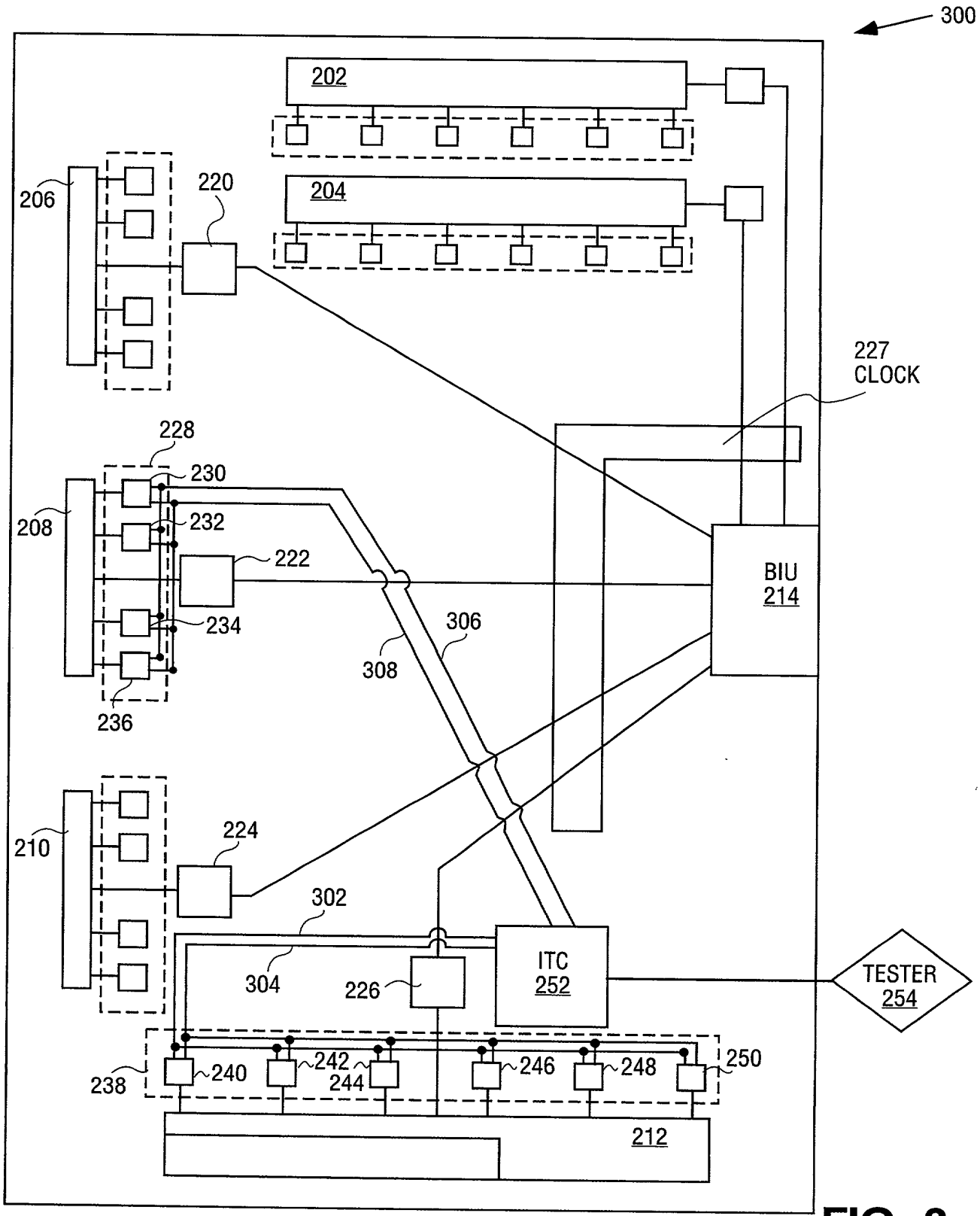

FIG. 3
(PRIOR ART)

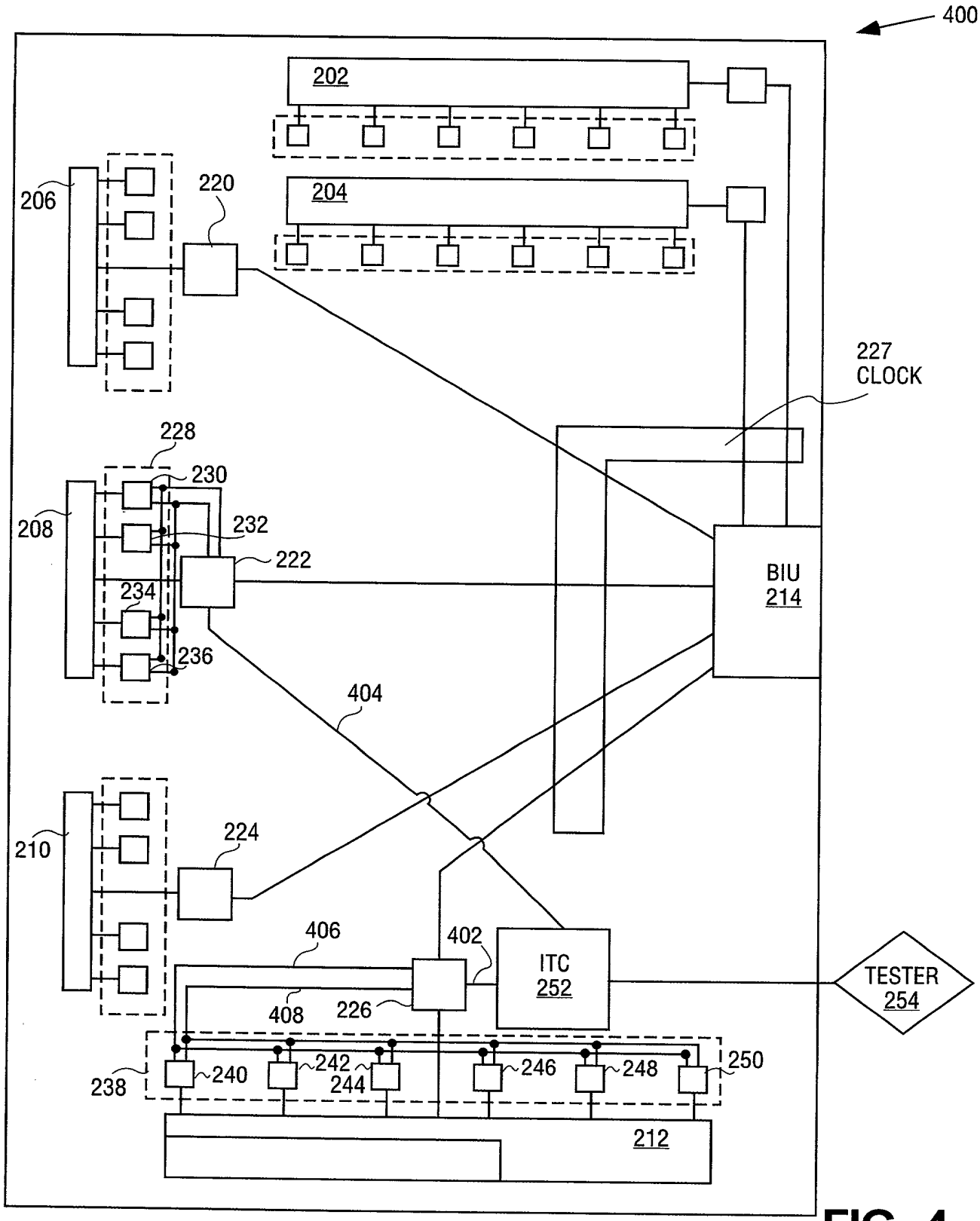
400
202
204
206
220
227
CLOCK
228
230
208
232
222
234
236
BIU
214
404
210
224
406
402
ITC
252
TESTER
254
408
226
238
240
242
244
246
248
250
212

FIG. 4

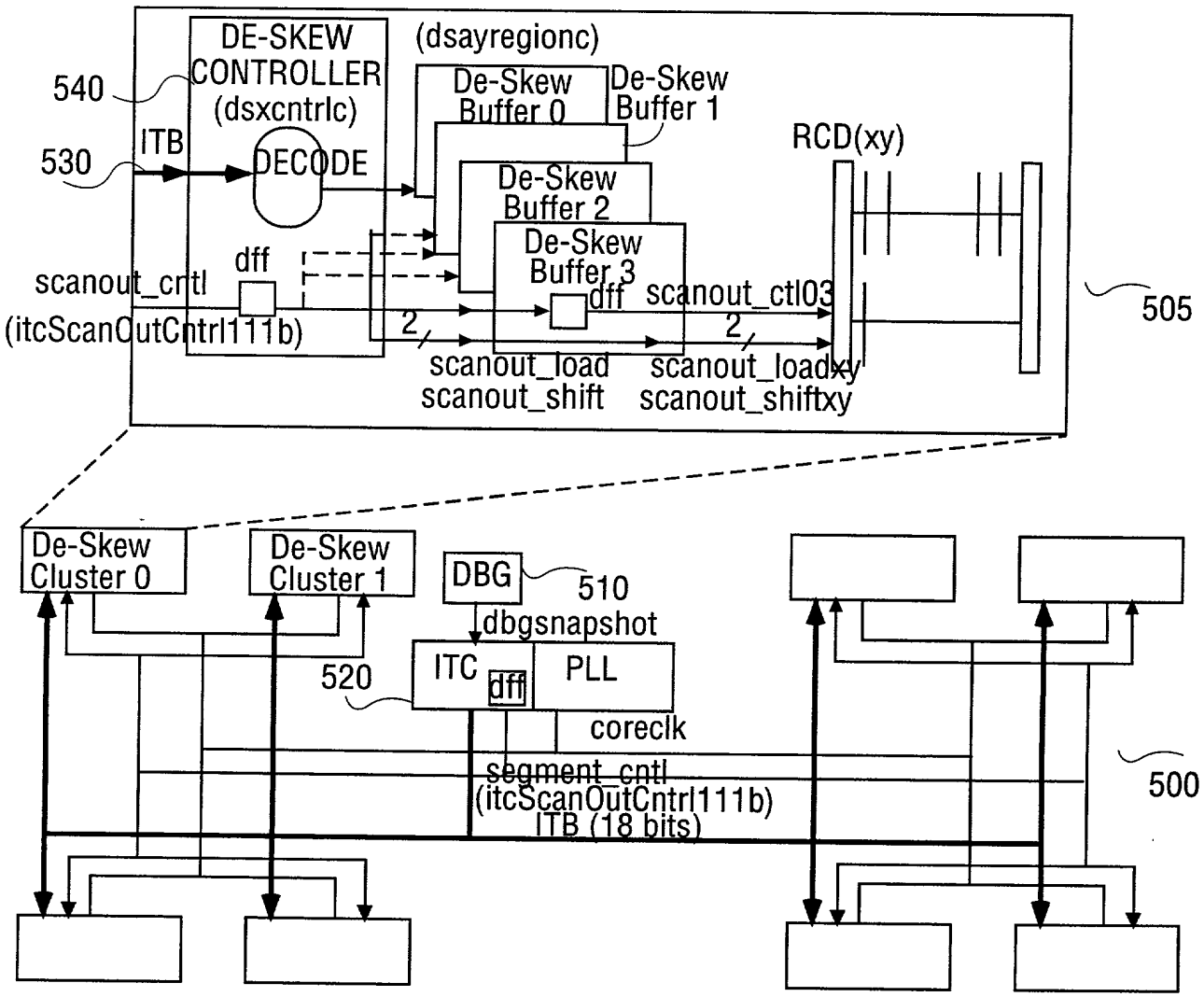
DE-SKEW
CONTROLLER
(dsxcntrlc)
(dsayregionc)
540
530
ITB
DECODE
De-Skew
Buffer 0
De-Skew
Buffer 1
De-Skew
Buffer 2
De-Skew
Buffer 3
RCD(xy)
dff
scanout_cntl
(itcScanOutCntrl111b)
2
dff
scanout_ctl03
2
scanout_load
scanout_shift
scanout_loadxy
scanout_shiftxy
505
De-Skew
Cluster 0
De-Skew
Cluster 1
DBG
510
dbgsnapshot
520
ITC
dff
PLL
coreclk
segment_cntl
(itcScanOutCntrl111b)
ITB (18 bits)
500

FIG. 5

control line/clock	Logic equations / details	Generated from	Driven to
scanout_load (non_critical)	SCANOUTSIG + SCANOUTLOAD + SCANOUTLOADDBG + (ISCAN_BUS + ISCAN_TAP)	De-skew controller	all LBFs
scanout_shift (non_critical)	SCANOUTSIG + SCANOUTSHIFT	De-skew controller	all LBFs
ck (clock driving scanout ff)	scanout_ctl & qclk	LBF	LBF
scanout_ctl	1. (SCANOUTLOADDBG & Run-test/Idle 2. (SCANOUTLOAD & Run-test/Idle & TDI) + 3. (SCANOUTSHIFT & (TCK & gclk)*) + 4. SCANOUTRST + 5. (SCANOUTSIG + Run-test/Idle & dbgsnapshot 6. (ISCAN_BUS + ISCAN_TAP)	ITC, staged in De-skew cluster	all LBFs

FIG. 6

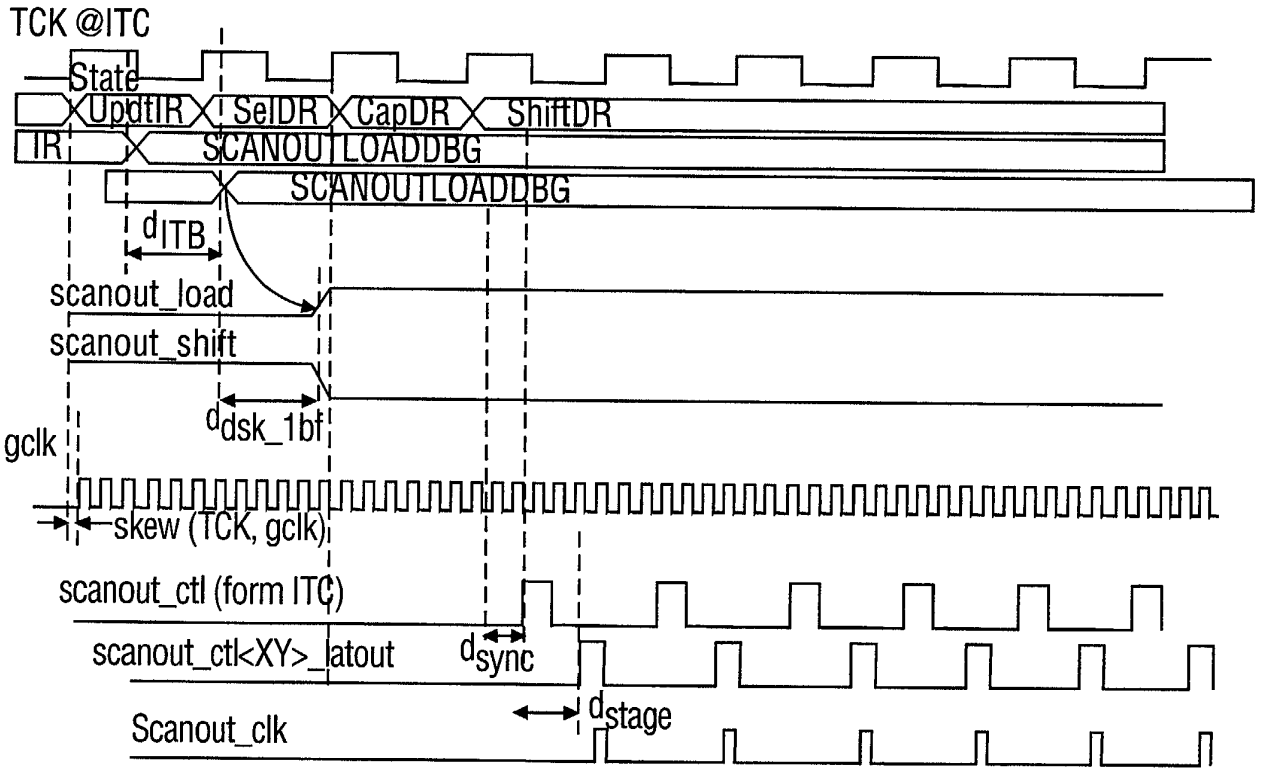
TCK @ITC
State
UpdtIR
SelDR
CapDR
ShiftDR
IR
SCANOUTLOADDBG
SCANOUTLOADDBG
dITB
scanout_load
scanout_shift
ddsk_1bf
gclk
skew (TCK, gclk)
scanout_ctl (form ITC)
scanout_ctl<XY>_latout
dsync
dstage
Scanout_clk

FIG. 7

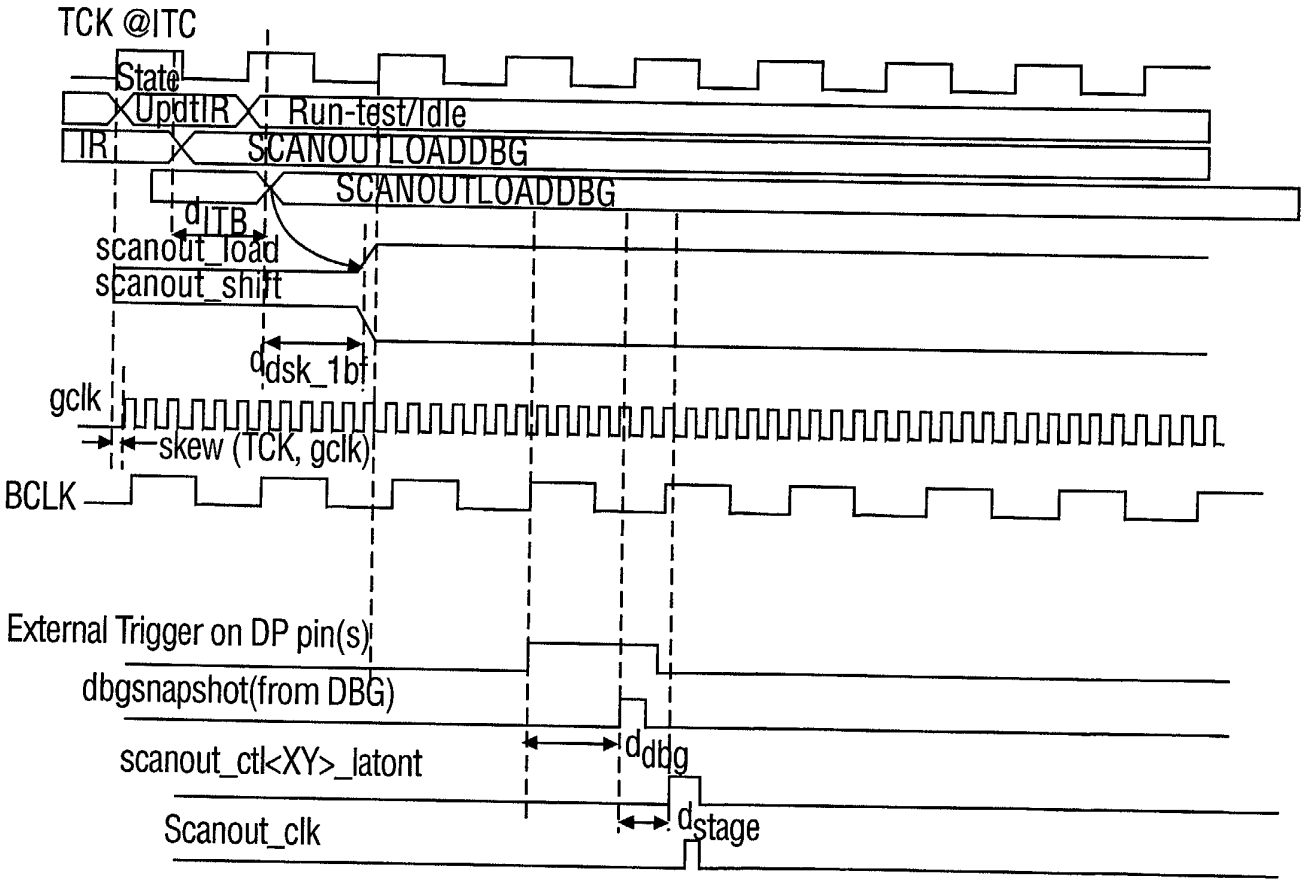
TCK @ITC
State
UpdtIR
Run-test/Idle
IR
SCANOUTLOADDBG
SCANOUTLOADDBG
dITB
scanout_load
scanout_shift
ddsk_1bf
gclk
skew (TCK, gclk)
BCLK
External Trigger on DP pin(s)
dbgsnapshot(from DBG)
scanout_ctl<XY>_latont
ddbg
Scanout_clk
dstage

FIG. 8